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501.43494X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Hiroki KANAI

Serial No.: 10/771,465

Filed: February 5, 2004

For: STORAGE DEVICE CONTROLLING DEVICE AND CONTROL METHOD FOR STORAGE DEVICE CONTROLLING DEVICE

RENEWED REQUEST FOR RECONSIDERATION OF PETITION TO MAKE SPECIAL UNDER 37 CFR 1.102(d) and MPEP. §708.02, VIII

MS Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

May 4, 2005

Sir:

1. Petition

Applicants hereby renews its Petition to make this application **Special** previously submitted on November 10, 2004, in accordance with 37 CFR §1.102(d) and MPEP 708.02, VIII. The November 10, 2004 Petition was denied by a Decision issued on April 4, 2005 in which the Petitions Examiner stated that the November 10, 2004 Petition failed to recite distinct features of the claimed subject matter. The present Request for Reconsideration of Petition incorporates by reference the November 10, 2004 Petition and provides additional details regarding the claims and how the claimed subject matter is patentable over the references. The present invention is a new application filed in the United States Patent and Trademark Office on February 5, 2004 and as such has not received any examination by the Examiner

2. Claims

Applicants hereby represent that all the claims in the present application are directed to a single invention. If upon examination it is determined that all the claims presented are not directed to a single invention, Applicants will make an election without traverse as a prerequisite to the granting of special status.

3. Search

Applicants hereby submit that a pre-examination search has been made by a professional searcher.

The field of search covered:

Class	Subclasses	Description
710/		ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
	8	. Peripheral configuration
711/		ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
	100	STORAGE ACCESSING AND CONTROL
	112	... Direct access storage device (DASD)
	117	. Hierarchical memories
	118	.. Caching
	147	. Shared memory area

The above subclasses represent areas deemed to contain subject matter of interest to one or more of the search features. Please note that relevant references may be classified outside of these areas. The integrity of the search is based on the records as presented to us by the United States Patent and Trademark Office (USPTO). No further integrity studies were

performed. Also a key word search was performed on the USPTO full-text database including published U.S. patent applications.

4. Copy of References

A listing of all references found by the professional searcher was provided by a Form PTO-1449 and copies of the references and the Form PTO-1449 were submitted as part of an Information Disclosure Statement (IDS) filed on November 10, 2004 (copy attached).

5. Detailed Discussion of the References and Distinctions Between the References and the Claims

Below is a discussion of the references uncovered by the search and cited in the IDS filed on November 10, 2004 (copy attached) that appear to be most closely related to the subject matter encompassed by the claims of the present application, and which discussion particularly points out how Applicants' claimed subject matter is distinguishable over those references. All other references uncovered by the search and cited in the IDS filed on November 10, 2004 (copy attached) are **not** treated in detail herein.

a. Detailed Discussion of the References

Chilton et al. (U.S. Patent No. 6,516,390 B1) provides for Methods and Apparatus for Accessing Data within a Data Storage System. The storage system as illustrated in Figs. 2 and 3 includes a buffer circuit 68-1 interconnected between a front end circuit 64-1 and a back-end circuit 66-1 residing on a circuit board 54-1 . The buffer circuit 68-1 includes a multi-port

memory 102 and cache interface logic 104. The buffer circuit 65-1 provides a direct path between the front-end and back-end circuits 64 and 66 (see column 5, lines 14-20; column 7, lines 6-8, 18-21, and 28-31; and column 9, lines 59-66 and Figs. 2 and 3).

Fukui et al. (U.S. Patent No. 6,646,947 B2) provides for a Data Transfer Control Device Semiconductor Memory Device and Electronic Information Apparatus. Discussed is a method and apparatus including a data transfer control device 11 as illustrated in Figs. 1 and 2 for controlling data transfer between first and second memory arrays based on an input control command and data transfer start addresses stored in the first and second memories and data transfer completion address output from a first address output section stored in the third memory section (see column 4, lines 25-49 and col. 8, lines 13-57).

Matsunami et al. (U.S. Patent Application Publication No. 2003/0023784 A1) provides for a Storage System Having a Plurality of Controllers. This application generally describes as illustrated in Fig. 1 a storage system 1 comprised of a plurality of disk array controllers 20, a plurality of file servers 30, a plurality of disk drive unit 41, a disk pool management unit 5 and a disk pool connection unit 61. The references teaches managing a larger storage area constituted by a plurality of drive units 41 constituting the large storage area as a disk pool 4. (see paragraphs 17-19 and 37 and 38).

Kobayashi et al. (U.S. Patent Application Publication No. 2004/0128456 A1) provides for a Storage System and Data Backup Method

for the same. As illustrated in Figs. 1 and 3 the storage system includes a network adapter 130 which includes a first processor 132 that receives a file access request and second processors that receive an access to data stored in the storage device, and a channel adapter which includes a third processor for sending data stored in the storage device, and a disk adapter for accessing data stored in the storage device (see paragraphs 31, 33-38, 53, and 54).

Tanaka et al. (U.S. Patent Application Publication No. 2004/0139168 A1) provides for a SAN/NAS Integrated Storage System. As illustrated in Figs. 1-4 and 6 a storage system 100 includes a channel adapter unit 110 for processing a command including block data and a file server unit 115 for processing a command including a file. The channel adapter unit 110 and file server unit 113 can be disposed on the same circuit board (file server board) 112 (see paragraphs 41, 43, 45 and 48-67 and Figs. 1-4 and 6).

Fujimoto et al. (JP 2003345515), assigned to Hitachi, Ltd. provides for a Disk Controller, Storage System, and Method for Controlling the same. A method of controlling transfer of data between a host and a cache memory, disk device and cache memory and a data transfer adapter means. The data transfer adapter reads the parameter stored in the memory and executes the transfer of data based on the read parameter.

b. Distinctions Between the References and the Claims

The present invention as recited in the claims is not taught or suggested by any of the above noted references whether taken individually or

in combination with each other or in combination with any of the other references now of record.

The present invention as now recited in the claims is directed to a storage controlling device, including a channel controller for receiving a data input/output request based on a file-name indication, a disk controller for carrying out input/output control of data stored in a storage volume, and a first memory for storing the data delivered between the channel controller and the disk controller.

The channel controller includes a first feature of a first processor for outputting a block-basis I/O request related to the data input/output request and controlling the first memory, a second feature of a file access processor which has a second processor and a second memory controlled by the second processor and serves to control the transmission/reception of the data input/output request and the data which is carried out with the information processing device, a third feature of a data transfer device for controlling data transfer between the first memory and the second memory, and a fourth feature of a third memory controlled by the first processor which are formed on a circuit board.

Each of the independent claims recites different operations being performed by the first and second processors and the data transfer device. For example, claim 1 recites that the second processor transmits information indicating the storage position of the data in the second memory to the first processor, the first processor writes into the third memory data transfer information containing information indicating the storage position of the data in

the first memory and information indicating the storage position of the data in the second memory, and the data transfer device reads out the data transfer information from the third memory and controls the data transfer between the first memory and the second memory based on the data transfer information. The other independent claims, namely claims 2-4, 6-11, 13 and 14, each recite that the first and second processors and the data transfer device perform operations different from the first and second processors and the data transfer devices as recited in claim 1.

The above described features namely the first, second, third and fourth features of the present invention included within the channel controller as recited in each of the independent claims of the present application are not taught or suggested by any of the references of record whether taken individually or in combination with each other.

For example, the above described first, second, third and fourth features included within the channel controller of the present invention as recited in each of the independent claims are not taught or suggested by Chilton. As described above, Chilton provides a storage system which includes a buffer circuit interconnected between front end and back end circuits. As taught by Chilton, the buffer circuit provides a direct path between the front end and back end circuits.

However, the teachings of Chilton do not anticipate or render obvious the above described first, second, third and fourth features included in the channel controller as recited in each of the independent claims. Therefore, the features of the present invention as recited in the claims are not taught or

suggested by Chilton.

The above described deficiencies of Chilton are also evident in each of the other references described above. Specifically, the above described first, second, third and fourth features included in the channel controller of the present invention as recited in each of the independent claims are not taught or suggested by any of the other references of record, namely Fukui, Matsunami, Kobayashi, Tanaka and Fujimoto whether taken individually or in combination with each other or in combination with Chilton.

For example, Fukui as described above teaches a data transfer control device 11 as illustrated, for example, in Fig. 1 which controls data transfer between first and second memory arrays.

However, the data transfer control device as taught by Fukui does not teach or suggest the above described first, second, third and fourth features included within a channel controller of the present invention as recited in each of the independent claims. Therefore, the features of the present invention as recited in the claims are not taught or suggested by Fukui.

Matsunami as described above includes a storage system having a plurality of disk controllers for accepting computer access through a Storage Area Network (SAN) and a plurality of file servers for accepting computer access through a LAN. Matsunami teaches, for example, a disk controller 20 as illustrated in Fig. 3 including fiber channel controllers 203, 204.

However, at no point is there any teaching or suggestion in Matsunami of a channel controller including the first, second, third and fourth features of the present invention as recited in each of the independent claims. Therefore,

the features of the present invention as recited in the claims are not taught or suggested by Matsunami.

Kobayashi as described above teaches, for example, a network adaptor 130 and a channel adaptor 140 wherein the channel adaptor includes an I/O processor for controlling input and output of data through a port 141. At no point is there any teaching or suggestion in Kobayashi that the channel adaptor 140 includes the above described first, second, third and fourth features as in the channel controller according to the present invention as recited in each of the independent claims. Therefore, the features of the present invention as recited in the claims are not taught or suggested by Kobayashi.

Tanaka as described above, teaches a storage system directly connected to a network having a channel adaptor 110. There is no teaching in Tanaka of the internal details of the channel adaptor 110.

Thus, at no point is there any teaching or suggestion in Tanaka that the channel adaptor 110 includes the first, second, third and fourth features of a channel controller according to the present invention as recited in each of the independent claims. Therefore, the features of the present invention as recited in the claims are not taught or suggested by Tanaka.

Fujimoto as described above teaches a disk controller having a channel adaptor part which includes a processor for controlling the transfer of data between a host and the cache memory. Fujimoto further teaches that the processor of the channel adaptor part stores a parameter for controlling the transfer of data in a memory in the processor.

However, at no point is there any teaching or suggestion in Fujimoto that the channel adaptor part includes the above described first, second, third and fourth features of the channel controller of the present invention as recited in each of the independent claims. Therefore, the features of the present invention as recited in the claims are not taught or suggested by Fujimoto.

Therefore, the above described first, second, third and fourth features of the channel controller of the present invention as recited in each of the independent claims are not taught or suggested by any of the references of record, namely Chilton, Fukui, Matsunami, Kobayashi, Tanaka and Fujimoto, whether taken individually or in combination with each other.

F. Conclusion

Applicant has conducted what it believes to be a reasonable search, but makes no representation that "better" or more relevant prior art does not exist. The United States Patent and Trademark Office is urged to conduct its own complete search of the prior art, and to thoroughly examine this application in view of the prior art cited herein and any other prior art that the United States Patent and Trademark Office may locate in its own independent search. Further, while Applicant has identified in good faith certain portions of each of the references listed herein in order to provide the requisite detailed discussion of how the claimed subject matter is patentable over the references, the United States Patent and Trademark Office should not limit its review to the identified portions but rather, is urged to review and consider the

entirety of each reference, and not to rely solely on the identified portions when examining this application.

In view of the foregoing, Applicant requests that this Petition to Make Special be granted and that the application undergo the accelerated examination procedure set forth in MPEP 708.02 VIII.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (501.43494X00).

Respectfully submitted,

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